REMARKS

Claims 1-18 are pending in the application. Claim 1 is canceled. Claims 8-18 are allowed. Claims 2-7 are rejected.

Claims 2-7 are rejected under 35 USC § 103(a) as being unpatentable over Osaka et al. (US Patent No. 6,034,878) in view of Yeager et al. (US Patent No. 5,802,583).

The office action states that " Osaka, et al....discloses...a plurality of memory modules of DRAM type 10-0 to 10-15 being arranged such that a control signal output from one memory module is electrically sequentially wired to another through connectors C6-1 and C6-2 (see lines 48-59, column 26; lines 52-61; column 27)..."

However, the text referenced is merely showing how the wiring is achieved, the control signals are not controlled such that "a control signal *output* from one device is electrically connected to a control signal *input* to a sequential device." See Osaka, column 27, lines 2-5, "As a result [of the wiring], it is possible to operate this source-clock-synchronized memory system as the same way as the first embodiment."

Referring to the text with regard to the first embodiment, it becomes apparent that the entire disclosure of Osaka is directed to arranging memory modules such that control signals, such as S1, S2 and S3 reach the modules at the same time, in a synchronized fashion. See Osaka, column 10, lines 35-39. In contrast, the control signals of the instant application are set up so that a particular control signal, data out, is wired to a particular control input, data in, of the next module. Claim 2 has been amended to more clearly show this.

In Osaka, the control signals propagate through memory modules but they are not actually asserted for each module in turn. See Osaka, column 10, line 49 through column 11, line 8. The system in Osaka addresses the propagation time as signals pass through distances equivalent from one module to the next, but do not actually assert the control signals sequentially, as is required by claim 2. Further, the control signals S1, S2 and S3 are the

same for each module is Osaka, they are not different signals, such as data in and data out, as in the instant application.

The addition of Yeager merely addresses the use of ferroelectric memories. Yeager does not overcome the deficiencies of Osaka with regard to the above discussion. It must be noted that polymer ferroelectric memories are vastly different than other types of ferroelectric memories.

It is therefore submitted that claim 2, as amended, is patentably distinguishable over the prior art and allowance of this claim is requested.

Claims 3-7 depend from claim 1 and should be ruled allowable for that reason and for their own merits.

No new matter has been added by this amendment. Allowance of all claims is requested. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Customer No. 32231

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

Julie L. Reed

Julie L. Reed
Reg. No. 35,349

MARGER JOHNSON & McCOLLOM, P.C.
1030 SW Morrison Street
Portland, OR 97205
(503) 222-3613